REMARKS

The status of the application is as follows. Claims 1-9 were presented for prosecution and stand rejected. Claims 1, 3, 6, and 9 have been amended herein. Claims 1, 6 and 9 were rejected under 35 USC 112, and have been amended herein to more definitely claim the subject matter of the invention. Claims 1-4, and 6-8 were rejected under 35 USC 102(b) as being anticipated by Kawaguchi (U.S. 5,739,573) "Kawaguchi." Claims 1, 5-6, and 9 were rejected under 35 USC 102(e) as being anticipated by Lur et al. (U.S. 6,013,569) "Lur." In addition, the specification was objected to for failing to include headings, which have been added herein by amendment to comply with the requirements of the Office. No new matter is believed added.

Applicants respectfully traverse the finding that independent claim 1 is anticipated by Kawaguchi and Lur. Kawaguchi fails to describe, *inter alia*, a trench that "comprises a depth that is maximally half the height of the larger isolation area." Rather, as can be seen in Figure 5F of Kawaguchi, the trench depth is greater than half the height of the larger isolation area. Accordingly, Kawaguchi fails to teach each and every claim element of claim 1.

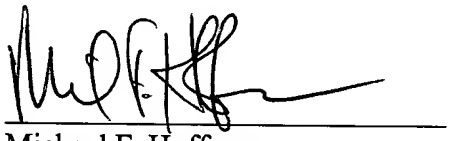
Lur fails to describe, *inter alia*, "a smaller isolation layer (402) that is formed by depositing an oxide layer over and around the polysilicon region in a single step." Rather, Lur describes a method in which "a sacrificial material 56 is first provided over the polysilicon layer 56," later followed by a thermal oxidation process in order "to grow a thin liner oxide layer 58 over the sides," see Lur, column 7, lines 5-50. Accordingly, Lur fails to teach forming a smaller isolation layer by depositing over and around the polysilicon in a **single step**. Because the two references fail to teach each and every

claim element of claim 1, Applicants respectfully submit that claim 1, and the claims that depend therefrom are in condition for allowance.

Applicants also respectfully traverse the finding that independent claim 6 is anticipated by Kawaguchi and Lur. Both Kawaguchi and Lur fail to teach, *inter alia*, an integrated circuit, "wherein the metal silicide includes a substantially planar surface that is above the larger isolation layer." A careful examination of both Kawaguchi and Lur shows a metal silicide surface that is **below** the larger isolation layer (see Figures 5F and 9 of the respective patents). Moreover, the silicide surface of Lur is not planar, but rather is concave in shape. Accordingly, because the two references fail to teach each and every claim element of claim 6, Applicants respectfully submit that claim 6, and the claims that depend therefrom are in condition for allowance.

If the Examiner believes that anything further is necessary to place the application in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number listed below.

Respectfully submitted,



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SEPARATE MARKUP SHEET

In the Claims

1. A method of manufacturing an integrated circuit, which method includes a stage wherein lateral isolation regions (spacers) are formed at the sides of a projecting polysilicon region so as to be in contact therewith, said lateral isolation regions each being composed of a smaller isolation layer (402) that is formed by depositing an oxide layer over and around the polysilicon region in a single step, which is in contact with said projecting region (2), and of a larger isolation layer, which method also includes a silicidation process to which the upper part of the polysilicon region is subjected, which silicidation process includes the deposition on said upper part of a metal layer which is capable of forming a metal silicide (5) with the silicon, characterized in that the silicidation process includes, prior to the deposition of said metal layer, an etch step to which at least the vertical portion of the smaller isolation layer (402) is subjected so as to form a trench (TR) [of predetermined depth (h)] between the larger isolation layer (411) of each lateral isolation region and the corresponding side (F) of the polysilicon region (2), wherein the trench comprises a depth that is maximally half the height of the larger isolation area, and in that the deposition of the metal layer is a directional deposition.

3. A method as in claim 1, characterized in that the depth (h) of the trench is equal to [maximally half the height (H1) of the larger isolation layer and] maximally half the thickness (E) of the larger isolation layer.

6. An integrated circuit comprising lateral isolation regions formed at the sides of a least one projecting region of polysilicon so as to be in contact therewith, each lateral isolation region being composed of a smaller isolation layer (402), contacting said projecting region (2), and a larger isolation layer (411), and comprising a zone (5) including a metal silicide situated in the upper part of the polysilicon region (2), characterized in that each lateral isolation region comprises a vertical trench (TR) made in the smaller isolation layer (402) between the larger isolation layer (411) and the corresponding side (F) of the projecting region (2), said trench (TR) extending from the top of the larger isolation layer (411) of the corresponding lateral isolation region down to a [predetermined] depth (h), and wherein the metal silicide includes a substantially planar surface that is above the larger isolation layer.

9. An integrated circuit as claimed in claim 6, characterized in that each lateral isolation region comprises a horizontal trench (TH) made in the smaller isolation layer (402) between a larger isolation layer (411) and the substrate (1) of the integrated circuit[, said trench extending from the lateral edge of the larger isolation layer of the lateral isolation region].